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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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08/921,250 08/29/97 INOUE

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EXAMINER

GOUDREAU, G

ART UNIT	PAPER NUMBER
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1765

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

08-921,250

Applicant(s)

Inoue et. al.

Examiner

George Goudreau

Group Art Unit

1765

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on (11/99 to 12/99) (i.e., papers # 6-7)

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-30 is/are pending in the application.

Of the above claim(s) 29-30 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-4, 9-16, 20-27 is/are rejected.

☒ Claim(s) 5-8, 17-19, 28 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Applicable Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All. ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 1.7.2(a)).

*Certified copies not received: _____

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 2, 7

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

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15. Claims 9, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-In claims 9, and 20, the wording "than 30 of purified water" is confusing, and should be rewritten.

16. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

18. Claims 1, 15-16, 22, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu et. al. (5,314,843).

Yu et. al. disclose a process for planarizing an SiO₂ insulating film on the surface of a semiconductor wafer which is comprised of the following steps:

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-First, a TEOS type SiO₂ film (46) is conformably formed on the surface of a Si semiconductor wafer (41) having multiple layers of insulators, and conductors (42) on its surface.;

-Second, B, and P ions are ion implanted selectively into a top portion of the SiO₂ layer (46) to form a BPSG region (44) in the surface of the SiO₂ layer (46).; and

-Third, the BPSG, and SiO₂ layers are cmp planarized using a slurry comprised of (KOH, H₂O, and silica abrasive particles).

This is discussed specifically in columns 6-8; and discussed in general in columns 1-12.

This is shown specifically in figures 5-7; and shown in general in figures 1-4, 8-10.

19. Claims 1-3, 11, 13-16, 22, and 24-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shepard (5,616,513).

Shepard discloses a process for forming a STI structure in a Si wafer which is comprised of the following steps:

-First, trenches are etched into the surface of a Si wafer using a patterned photo resist/Si₃N₄/SiO₂ multi-layered structure as an etch mask.;

-Second, a SiO₂ layer is conformably deposited into trenches formed in the surface of a Si wafer, and onto the surface of the Si₃N₄/SiO₂ multi-layered structure located outside the trenches.;

-Third, P ions are ion implanted into the top surface of the SiO₂ layer.;

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-Fourth, a SiO₂ layer is conformably deposited onto the surface of the P doped SiO₂ layer.; and

-Fifth, the SiO₂, and P-doped SiO₂ layers are cmp polished down to the surface of the Si₃N₄ layer.

This is discussed specifically in columns 3-5; and discussed in general in columns 1-6.

This is shown specifically in figures 4A-4C; and shown in general in figures 1-3, 5.

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

21. Claims 20-21, 23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference as applied in paragraph 18 above.

The reference as applied in paragraph 18 above fail to specifically disclose the following aspects of applicant's claimed invention:

-the formation of an insulating film with the specific wetting properties claimed by the applicant;

-the use of an SOG precursor to form the SiO₂ layer out of in place of the TEOS precursor used to form the SiO₂ layer out of; and

-the use of a surfactant of the type claimed by the applicant (IE.- a fatty acid surfactant) in the cmp slurry used to planarize the BPSG/SiO₂ layers in the process taught above

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It would have been obvious to one skilled in the art to replace the SiO₂ layer formed from a TEOS precursor in the process taught above with a SiO₂ layer formed from an SOG precursor based upon the following. First, this would simply represent an alternative, and at least equivalent means for forming the SiO₂ layer in the process taught above to those means specifically taught. Second, the usage of a SOG precursor to form a SiO₂ layer on a semiconductor wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.)

It would have been obvious to one skilled in the art to use a surfactant of the type claimed by the applicant (IE. -a fatty acid surfactant) in the cmp polishing slurry used to planarize the BPSG/SiO₂ layers in the process taught above based upon the following. The usage of surfactants in cmp slurries used to planarize layers on a semiconductor substrate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) It would have been obvious to one skilled in the art to use any of a variety of different types of surfactants in the cmp slurry taught above including fatty acid type surfactants based upon the following. The usage of fatty acid surfactants in cmp slurries used to planarize layers on a semiconductor wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.)

It would have been prima facie obvious to form insulating layers on the semiconductor wafer in the process taught above which have any of a variety of different wetting angles including those claimed by the applicant. These are all well known variables in semiconductor fabrication

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arts which are known to effect both the properties of the fabricated device. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

22. Claims 4, 9-10, 12, 20-21, 23, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference as applied in paragraph 19 above.

The reference as applied in paragraph 19 above fail to specifically disclose the following aspects of applicant's claimed invention:

- the formation of an insulating film with the specific wetting properties claimed by the applicant;
- the use of an SOG precursor to form the SiO₂ layer out of in place of the TEOS precursor used to form the SiO₂ layer out of;
- the use of a surfactant of the type claimed by the applicant (IE.- a fatty acid surfactant) in the cmp slurry used to planarize the BPSG/SiO₂ layers in the process taught above; and
- the usage of a CVD deposition process to deposit the SiO₂ layers onto the wafer in the process taught above.

It would have been obvious to one skilled in the art to use a CVD process to form any of the SiO₂ layers in the process taught above using a TEOS precursor based upon the following. The usage of CVD processes to form SiO₂ layers on a semiconductor wafer from a TEOS precursor is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.)

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Alternatively, it would have been obvious to one skilled in the art to replace the SiO₂ layer formed from a TEOS precursor in the process taught above with a SiO₂ layer formed from an SOG precursor based upon the following. First, this would simply represent an alternative, and at least equivalent means for forming the SiO₂ layer in the process taught above to those means specifically taught. Second, the usage of a SOG precursor to form a SiO₂ layer on a semiconductor wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.)

It would have been obvious to one skilled in the art to use a surfactant of the type claimed by the applicant (IE, a fatty acid surfactant) in the cmp polishing slurry used to planarize the BPSG/SiO₂ layers in the process taught above based upon the following. The usage of surfactants in cmp slurries used to planarize layers on a semiconductor substrate is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) It would have been obvious to one skilled in the art to use any of a variety of different types of surfactants in the cmp slurry taught above including fatty acid type surfactants based upon the following. The usage of fatty acid surfactants in cmp slurries used to planarize layers on a semiconductor wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.)

It would have been prima facie obvious to form insulating layers on the semiconductor wafer in the process taught above which have any of a variety of different wetting angles including those claimed by the applicant. These are all well known variables in semiconductor fabrication

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arts which are known to effect both the properties of the fabricated device. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.


23. Claims 5-8, 17-19, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.


25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Benjamin Utech, can be reached on (703) -308-3836. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -308-3599.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.


George A. Goudreau/gag

Examiner AU 1765


**THI DANG
PRIMARY EXAMINER
GROUP 1700**